Code No: F-13635/N/AICTE

FACULTY OF ENGINEERING

B.E. (ECE/CSE/CME/AI&DS/AI&ML/IT) III-Semester (AICTE) (Main & Backlog) (New) Examination, February/ March 2024

Subject: Digital Electronics

Time: 3 Hours **Max. Marks: 70**

Note: (i) First question is compulsory and answer any four questions from the remaining six questions. Each question carries 14 Marks.
(ii) Answer to each question must be written at one place only and in the same order as they occur in the question paper.
(iii) Missing data, if any, may be suitably assumed.

1. a) Differentiate between variables and function.
   b) Diagrammatically show the implementation 1X8 demultiplexer using 1X4 demultiplexer.
   c) Give the block diagram of a comparator and state the inputs & outputs.
   d) Illustrate and explain the timing diagram of a 4-bit ring counter.
   e) Explain the Mealy FSM using a diagram.
   f) Illustrate the serial-in-parallel-out shift register with DFF.
   g) Explain the race-around condition.

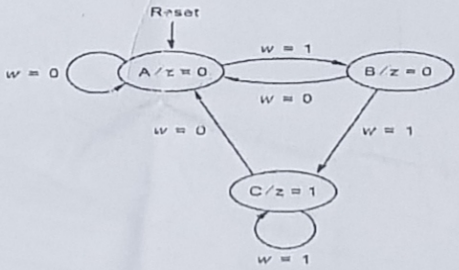
2. a) Simplify the function using Quine McClusky method
   $F(A,B,C,D)=\Sigma m(0,2,4,6,7,9)+\Sigma m(10,11)$ and realize the function with basic gates.
   b) Simplify the expressions using Boolean algebra.
   (i) (A+B) (A+B′) (A′+C) (ii) xyz′+x′yz+xyz+x′yz.

3. a) Design and implement a 4-to-2 binary Priority Encoder.
   b) Design and implement a Binary to Gray code converter.

4. a) Draw the 3-input LUT and explain.
   Program the LUT to implement the logic function $F = X_1X_2'X_3$ where X_1 is the MSB.
   b) Draw and explain the structure of the CPLD.

5. a) Convert the TFF to JKFF.
   b) Design and implement a 3-bit Synchronous counter using TFF.

6. a) Explain in detail the design and operation of a universal bi-directional shift register.
   b) Give the state table & ASM chart for the following



7. a) Give the complete steps involved in simplifying Boolean expressions using Karnaugh's Map. Illustrate using 4-variable K-map.
   b) Design and implement a 4-bit parity checker circuit.

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