Code No: 18070/BL

FACULTY OF ENGINEERING

BE IV-Semester (ECE) (AICTE) (Main & Backlog) Examination, October 2021

Subject: Computer Organization & Architecture

Time: 3 Hours | Max marks: 70

Missing data, if any, may be suitably assumed

PART – A

Note: Answer any five questions (5x2=10 Marks)

1. Show the hardware for Booth's [illegible]
2. Draw IEEE 754 formats of floating point representation.
3. What is direct and indirect address instructions
4. What is stack [illegible] organization?
5. Distinguish between RISC & CISC processors.
6. What is the role of [illegible] and [illegible]?
7. Compare and contrast between synchronous and asynchronous communication.
8. Explain the need for an I/O interface.
9. Distinguish between SRAM and Associative memory.
10. Explain the terms [illegible], index and [illegible] in relation to cache memory.

PART – B

Note: Answer any four questions. (4x15=60 Marks)

11. (a) Draw the flow chart for signed [illegible] and also draw the hardware [illegible] for that.
    (b) Differentiate between Restoring and Non Restoring division algorithm.

12. (a) Explain the [illegible] of computers [illegible].
    (b) Explain various [illegible] in detail.

13. (a) Explain [illegible] with [illegible] technique.
    (b) What is the [illegible] data transfer [illegible] without an interrupt?

14. (a) Explain the operation of daisy chaining method of priority interrupt.
    (b) What are the merits and demerits of programmed I/O data transfer?

15. (a) Explain Set Associative mapping in detail.
    (b) Explain the virtual memory in details.

16. (a) Describe in detail about IOP organization.
    (b) Explain the [illegible] cycle with flow chart.

17. (a) Explain the design of control unit. How to decode the micro operation fields? Explain the process.
    (b) Explain Vector processing in detail.

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