Code No: E-5688/N/BL/AICTE

FACULTY OF ENGINEERING

B.E. (ECE) IV Semester (AICTE) (Main & Backlog) (New) Examination, September / October 2023

Subject: Computer Organization and Architecture

Time: 3 Hours **Max. Marks: 70**

Note: (i) First question is compulsory and answer any four questions from the remaining six questions. Each questions carries 14 Marks.
(ii) Answer to each question must be written at one place only and in the same order as they occur in the question paper.
(iii) Missing data, if any, may be suitably assumed.

1. a) Draw and explain single and double precision IEEE 754 format.
   b) Convert $(+132.12)_{10}$ into normalized floating-point binary.
   c) Write a short note on Vector Processing.
   d) Map the Physical Address 4FFECF in to Cache Address in Associative Mapping.
   e) Explain strobe control signaling in asynchronous data transfer.
   f) Differentiate between RISC and CISC processors.
   g) Define Address Space and Memory Space.

2. a) Draw and explain IAS stored program model with features and illustrate in steps for storing and executing an instruction.
   b) Explain Non-restoring division algorithm with an example.

3. a) Explain microprogrammed address sequencer with neat diagram.
   b) Draw Instruction cycle and explain it with timing and Control.

4. a) For T = (A*B)+(C*D) write program using different operand length in an instruction n format and justify with Instruction cycle and Program execution time.
   b) Write a short note on stack organization and solve (3*2)+(4*2) using stack with neat diagram.

5. a) Explain different priority interrupt techniques with neat diagram.
   b) Explain DMA controller and transfer.

6. a) Brief paging system in virtual mapping and explain address mapping using pages.
   b) Describe the concepts of Cache organization and explain Associative Mapping.

7. a) Explain Instruction pipeline and brief different hazards in instruction pipelining.
   b) Draw and explain Floating point Addition and Subtraction block diagram.

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